REMARKS

The rejections and comments of the Examiner set forth in the Office Action dated April 10, 2003 have been carefully reviewed by the Applicants. Claims 16-35 are currently pending, with Claims 16-35 being rejected. Independent Claims 16 and 19 have been amended.

Claims 19 and 28-35 are currently rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the invention. Specifically, the recitation of "self-limiting diffusion process" is not provided in the disclosure. In response, the term "self-limiting" has been replaced by the term "corner-limiting." As pointed out by the Examiner, the disclosure refers to a "corner-limiting diffusion process."

Claims 16, 17, 21, 24, 25, and 27 are rejected under 35 U.S.C. 102(b) as being anticipated by Acovic (US 5315142). In response, Independent Claim 16 has been amended to recite "forming sidewall dopings on the sidewalls to reduce coupling between the control gate and the source and drain regions." Acovic neither teaches nor suggests the forming of sidewall dopings on the sidewalls of the trench to reduce coupling between the control gate and the source and drain regions.

Among the cited references, Lin has been relied upon as teaching "sidewall doping" and used in combination with Acovic. One with normal skill in the art would not find motivation to combine Lin with Acovic in either reference. Acovic and the present invention are directed to horizontal transistor devices, in which the current flow is in channel underneath the bottom of the trench. Lin is directed to a vertical transistor device, with a channel that is adjacent to the sidewalls, not underneath the bottom of the trench. The sidewall doping of the present invention is used to reduce coupling between the source and drain regions and the control gate, not adjust the threshold voltage (see page 3, lines 16-18). Lin teaches an implant to adjust threshold voltage in a vertical device and does not teach an implant to decouple the source and drain from the control gate.

The implant of the sidewalls in the present invention has nothing to do with the threshold voltage, as the channel is at the bottom of the trench. Since none of the references cited, separately or in combination, teach the invention as claimed in amended independent Claim 16, Applicants assert that Claims 16-18 and 20-27 are now in condition for allowance.

Claim 19 is currently rejected under 35 U.S.C. 103(a) as being unpatentable over Acovic (US 5315142) in view of Kroger (US 4544937). The Applicants respectfully traverse the rejection on the grounds that there is no motive to combine Acovic and Kroger in the manner described in the rejection, and also on the grounds that the combination of Acovic and Kroger fails to teach each and every element of amended Claim 19.

The rejection holds that "Kroger, on the other hand, teaches that diffusion and ion-implantation processes are equivalent doping techniques, both well know in the art (col. 6/ll.24-28)." This is incorrect. Kroger teaches that "Suitable methods of production of the degenerately doped regions include standard planar diffusion techniques and ion implantation followed by annealing." Kroger merely states degenerately doped regions may be produced by either method. One with normal skill in the art would know that it is extremely difficult to obtain the same dopant profile with diffusion and implantation, due to the fundamentally different mechanisms of the two processes. The two processes cannot be deemed equivalent when each is capable of achieving doping profiles that the other cannot, and when it is also extremely difficult to obtain the same profile using the two processes individually.

Kroger never uses any terminology that would suggest that the two processes are "equivalent" as maintained by the Examiner, and in fact describes ion implantation as an "alternative method" and directly contrasts diffusion and implantation processes at column 6, lines 62-67.

Claim 19 has been amended to recite a "corner-limiting process." As described in the specification, corner limiting is a result of the trench corner providing an obstacle that prevents diffusing species from traveling in a direct path. The "self-limiting diffusion" referred to in the rejection, and described by Kroger, is based upon the limiting effects of controlling the amount of dopant available for diffusion, and not based upon an obstacle to the diffusing species. Thus, as has been pointed out in the

earlier rejection under 35 U.S.C. 112, self-limiting diffusion and "corner-limiting diffusion" are distinct processes. The Applicants assert that amended Claim 19 and dependent Claims 28-35 are now in condition for allowance.

Independent Claims 16 and 19 have been amended to clearly distinguish Claims 16-35 over the cited references both individually, and collectively. In summary, the Applicants assert that Claims 16-35 are in condition for allowance, and earnestly solicit such action by the Examiner.

Please charge any additional fees or apply any credits to our PTO deposit account number: 23-0085.

Respectfully submitted,

WAGNER, MURABITO & HAO

Date: July 9, 2003

Mehlin Dean Matthews
Registration Number: 46,127

WAGNER, MURABITO & HAO
Two North Market Street
Third Floor
San Jose, CA 95113

408-938-9060

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claim 16 has been amended as follows:

16. A method for fabricating a semiconductor device with a trenched gate comprising:

forming an oxide layer on the surface of a semiconductor substrate;

forming a nitride layer on said oxide layer;

etching a trench having substantially upright vertical sidewalls and a bottom surface in said semiconductor substrate;

~~forming a trench-to-gate insulating layer inside the trench, wherein the trench-~~ to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a trench gate tunneling dielectric formed on the bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath the bottom of the trench;

forming sidewall dopings on the sidewalls to reduce coupling between the control gate and the source and drain regions;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode; and

forming a control gate electrode on a top surface of the inter-gate dielectric layer.

Claim 19 has been amended as follows:

19. A method for fabricating a semiconductor device with a trenched gate comprising:

etching a trench having substantially upright vertical sidewalls and a bottom surface in a semiconductor substrate;

forming a trench-to-gate insulating layer inside the trench, wherein the trench-to-gate insulating layer comprises a trench gate dielectric spacer formed on the upright vertical sidewalls inside the trench and a ~~trench gate tunneling dielectric formed on the~~ bottom surface inside the trench;

forming a trenched gate electrode on the trench-to-gate insulating layer inside the trench;

forming a source region and a drain region in the semiconductor substrate such that the source and drain regions partially extend laterally underneath the bottom of the trench;

forming an inter-gate dielectric layer on a top surface of the trenched gate electrode;

forming a control gate electrode on a top surface of the inter-gate dielectric layer, and

wherein the step of forming a source region and a drain region comprises a [self-limiting] corner-limiting diffusion process.